

***Allowable Subject Matter***

1. Claims 2-6 are allowed.

***Reasons for Allowance***

2. The following is an examiner's statement of reasons for allowance:

The prior art taken singly or in combination does not teach or suggest, a video signal processing circuit, among other things, comprising:

*said control means unit comprises a delay unit which delays and inputs a display read control signal and a data latch signal for said predetermined delay time during a period which is after a point at which said memory clock signal corresponding to writing of said pixel data in said GRAM is supplied, said writing accompanying said contention, but which is before supplying of the next memory clock signal following said memory clock signal so that said latch circuit reads pixel data corresponding to pixels representing said scanning line (claim 2);*

*when writing of said pixel data in said GRAM is executed plural times during a contention-free memory update period in which said pixel data corresponding to said pixels representing said scanning line are read to said latch circuit from said GRAM said control means unit upon occurrence of said contention delays reading of said pixel data corresponding to said pixels representing said scanning line between a period of writing said pixel data and a period of writing next pixel data, and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM again plural times during said contention-free memory update period (claim 6).*

The closest prior art, Ikeda (U.S. Patent No. 6,734,863) fails to teach the above features.

Art Unit: 2628

***Conclusion***

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

/Hau H Nguyen/

Primary Examiner, Art Unit 2628